

Highly Integrated Offline Current Mode PWM Power Switch

■ Description

FS6107D is a high performance current mode PWM power switch for offline flyback converter applications.

In FS6107D, PWM switching frequency with shuffling is fixed to 65KHz and is trimmed to tight range. The IC has built-in green and burst mode control for light and zero loadings, which can achieve less than 75mW standby power .

FS6107D integrates functions and protections of Under Voltage Lockout (UVLO), VDD over Voltage Protection (VDD OVP), Cycle-by-cycle Current Limiting (OCP), Short Load Protection (SLP), Over Load Protection (OLP), On-Chip Thermal Shutdown (OTP), Soft Start, VDD Clamping, etc.

■ Features

- Control Supports DCM and CCM Operation
- $\pm 1\%$ CV Regulation with Fast Dynamic Response
- Less than 75mW Standby Power
- Current Mode Control
- Built -in Frequency Shuffling
- Fixed 65KHz Switching Frequency
- Green Mode and Burst Mode Control
- On-chip Thermal Shutdown
- Cycle -by-Cycle Current Limiting
- Built -in Leading Edge Blanking
- Built -in Slope Compensation
- Very Low Startup and Operation Current
- Package: DIP-8

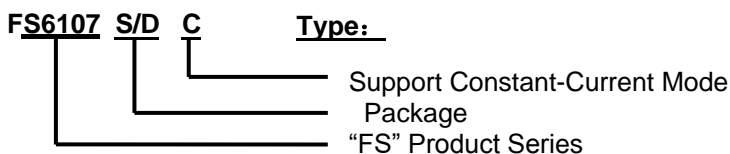
■ Applications

- Chargers and Adapter
- Motor Driver Power Supply
- Recommended Output Power⁽¹⁾

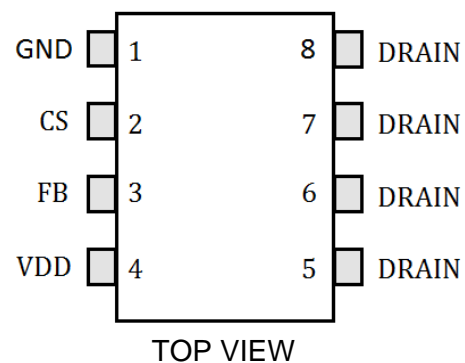
Part Number	90~264Vac	175-264Vac
FS6107D	24W	36W

Note 1: Typical continuous power in a non-ventilated enclosed adapter with sufficient drain pattern as a heat sink at 40 °C ambient.

■ Ordering Information

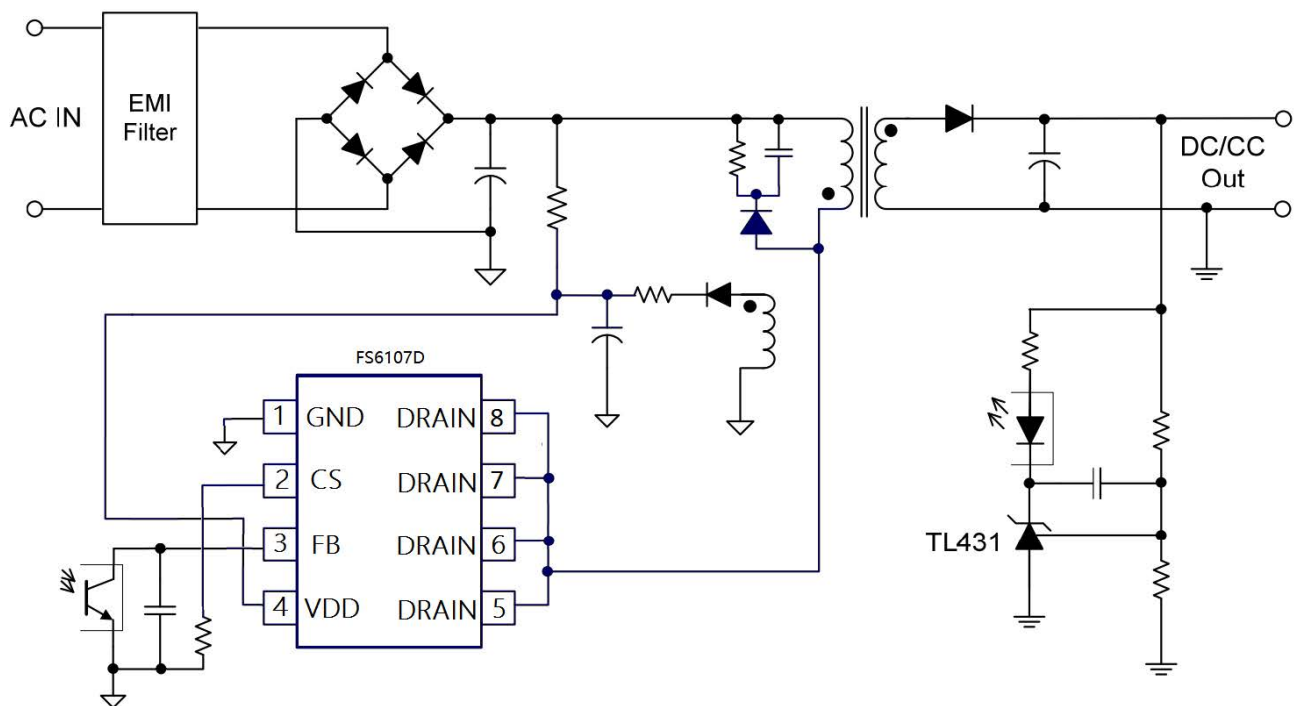


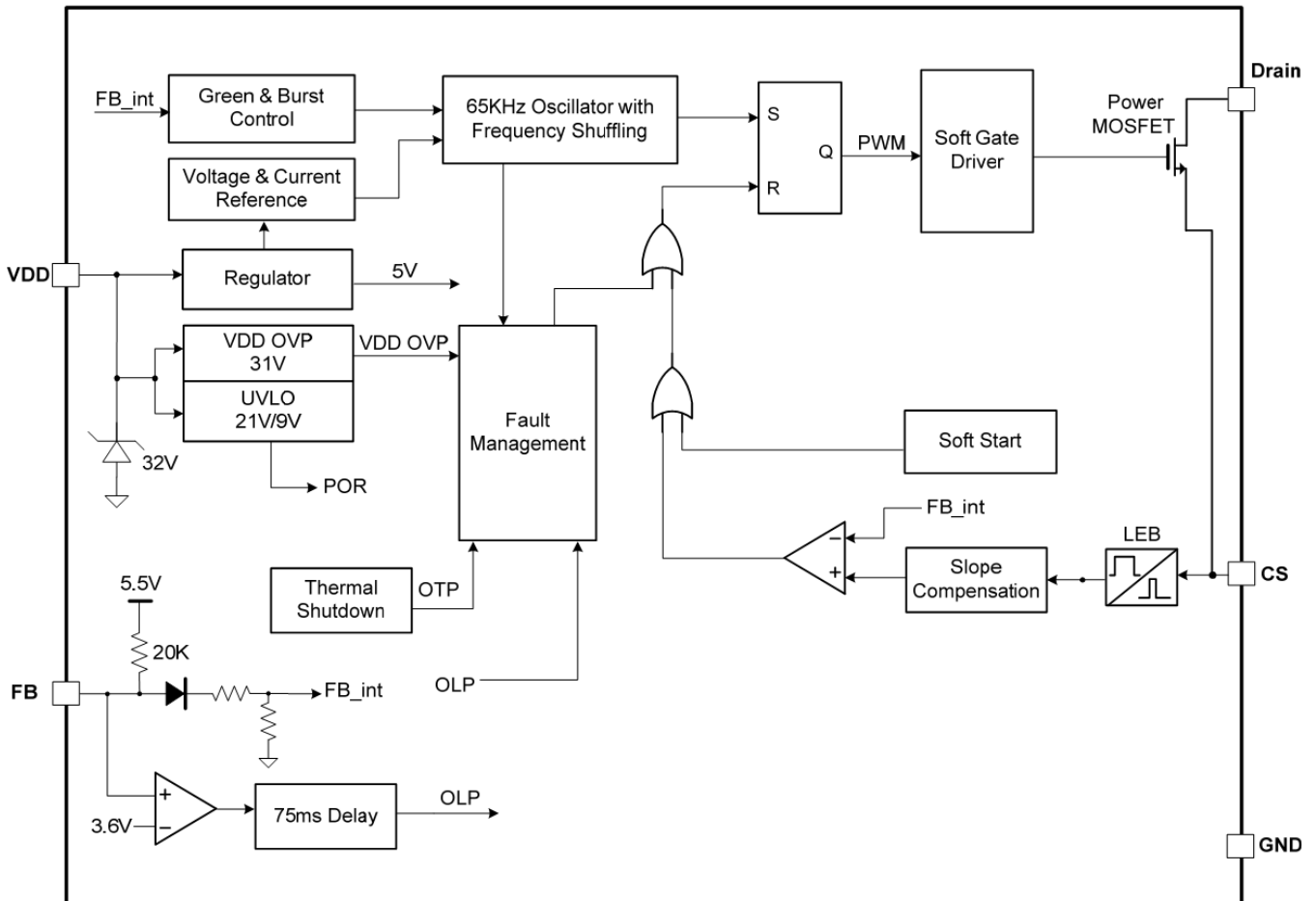
■ Package Information



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Pin Configuration

Pin Number	Pin Name	Function
1	GND	The ground of the IC.
2	CS	Current Sense Input Pin.
3	FB	Feedback pin. The loop regulation is achieved by connecting a photocoupler to this pin. PWM duty cycle is determined by this pin voltage and the current sense signal at Pin 4.
4	VDD	IC power supply pin.
5/6/7/8	DRAIN	The Power MOSFET Drain.

Typical Application Circuit


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■ Block Diagram

■ Absolute Maximum Ratings(Note 1)

Parameter	Value	Unit
VDD DC Supply Voltage	30	V
VDD DC Clamp Current	10	mA
FB, CS voltage range	-0.3 to 7	V
DRAIN voltage range	-0.3 to 650	V
Package Thermal Resistance (Junction to Ambient SOP-7)	165	°C/W
Package Thermal Resistance (Junction To Ambient DIP-7)	105	°C/W
Maximum Junction Temperature	175	°C
Storage Temperature Range	-65 to 150	°C
Lead Temperature (Soldering, 10sec.)	260	°C
ESD Capability, HBM (Human Body Model)	4	kV
ESD Capability, MM (Machine Model)	500	V



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■ Recommended Operation Conditions (Note 2)

Parameter	Value	Unit
Supply Voltage, VDD	10 to 26	V
Operating Ambient Temperature	-40 to 85	°C

■ Electrical Characteristics ($T_A = 25^\circ\text{C}$, VDD=20V, if not otherwise noted)

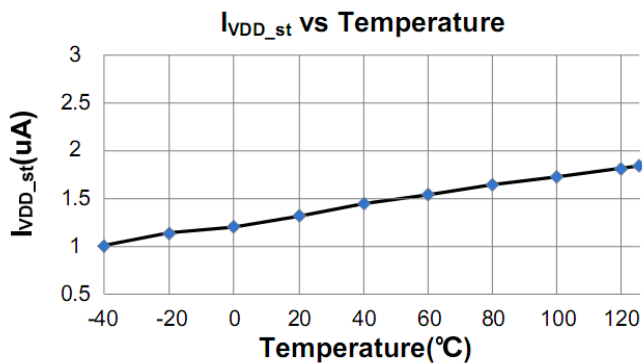
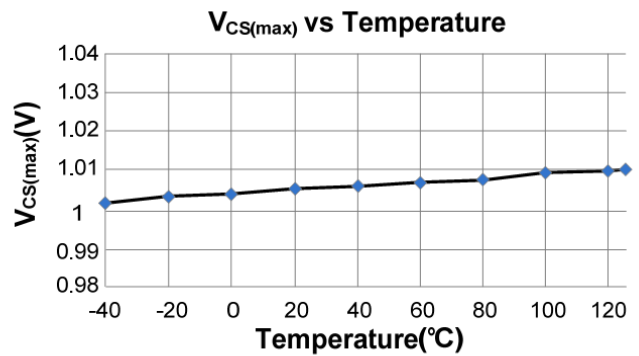
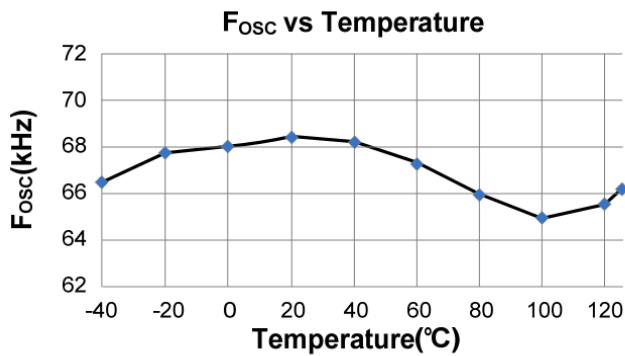
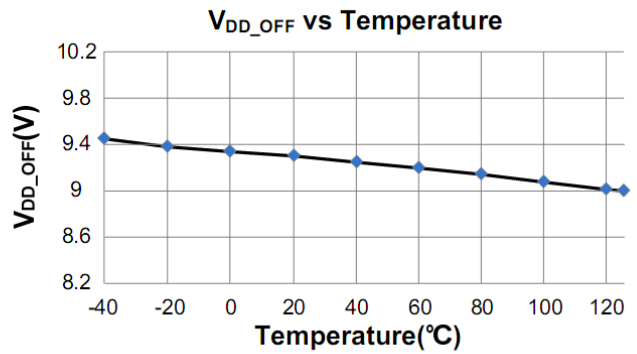
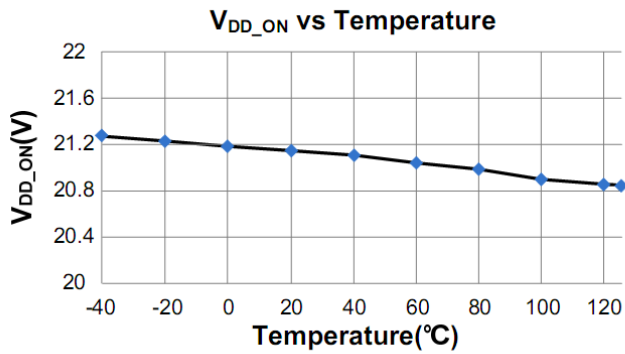
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
Supply Voltage Section(VDD Pin)						
I _{VDD_st}	Start-up current into VDD pin			2	20	uA
I _{VDD_op}	Operation Current	V _{FB} =3V,GATE=1nF		1.2	2	mA
I _{VDD_standby}	Standby Current			0.6	1	mA
V _{DD_ON}	VDD Under Voltage Lockout Exit		19	21	22.5	V
V _{DD_OFF}	VDD Under Voltage Lockout Enter		8	9	10	V
V _{DD_OVP}	VDD OVP Threshold		29	31	33	V
V _{DD_Clamp}	VDD Zener Clamp Voltage	I(V _{DD}) = 7 mA	33	35	37.5	V
Feedback Input Section (FB Pin)						
V _{FB_Open}	FB Open Voltage			5.5		V
I _{FB_Short}	FB Short Circuit Current	Short FB Pin to GND, Measure Current		0.3		mA
Z _{FB_IN}	FB Input Impedance			20		Kohm
A _{CS}	PWM Gain	$\Delta V_{FB} / \Delta V_{CS}$		2.0		V/V
V _{skip}	FB Under Voltage GATE Clock is OFF			1.0		V
V _{TH_OLP}	Power Limiting FB Threshold Voltage			3.6		V
T _{D_OLP}	Power Limiting Debounce Time			75		ms

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Current Sense Input Section (CS Pin)						
T_{LEB}	CS Input Leading Edge Blanking Time			250		ns
$V_{CS(max)}$	Current limiting threshold		0.97	1.0	1.03	V
T_{D_OC}	Over Current Detection and Control Delay	GATE=1nF		70		ns
Oscillator Section						
F_{OSC}	Normal Oscillation Frequency		60	65	70	KHz
$\Delta F(\text{shuffle})/F_{OSC}$	Frequency Shuffling Range		-4		4	%
T(shuffle)	Frequency Shuffling Period			32		ms
D_{MAX}	Maximum Switching Duty Cycle			66.7		%
F_{Burst}	Burst Mode Base Frequency			22		KHz
	Debounce Time					
On-Chip Thermal Shutdown						
T_{SD}	Thermal Shutdown	(Note 3)	---	165	--	°C
T_{RC}	Thermal Recovery	(Note 3)		140	--	°C
Power MOSFET Section (DRAIN Pin)						
BV_{DSS}	Power MOSFET Drain Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	650			V
R_{dson}	Static Drain-Source On Resistance	FS6107D, $V_{GS}=10V, I_D=3.5A$		1.2		Ω

Note:

1. Stresses listed as the above "Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to maximum rating conditions for extended periods may remain possibility to affect device reliability.
2. The device is not guaranteed to function outside its operating conditions.
3. Guaranteed by the Design.

Highly Integrated Offline Current Mode PWM Power Switch
■ Characterization Plots


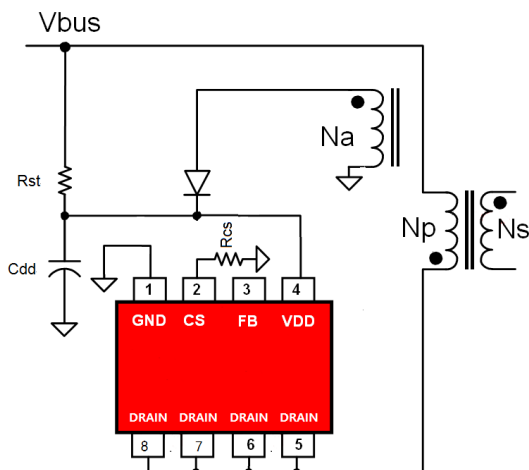
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■ Peration Description

FS6107D is a high performance current mode PWM power switch for offline flyback charger, motor driver power supply, and adapter applications.

● System Start-Up Operation and IC Operation Current

Before the IC starts to work, it consumes only startup current (typical 2uA) which allows a large value startup resistor to be used to minimize the power loss and the current flowing through the startup resistor charges the VDD hold-up capacitor from the high voltage DC bus. When VDD reaches V_{DD_ON} (typical 21V), FS6107D begins switching and the IC operation current is increased to be 1.2mA (typical). The hold-up capacitor continues to supply VDD before the auxiliary winding of the transformer takes the control of VDD voltage. When the IC enters into burst mode, the IC operation current will decrease further, thus less than 75mW standby power can be achieved.



● Oscillator with Frequency Shuffling

PWM switching frequency in FS6107D is fixed to 65KHz and is trimmed to tight range. To improve

system EMI performance, FS6107D operates the system with 4% frequency shuffling around setting frequency.

● Built-in Slope Compensation

In the conventional application, the problem of the stability is a critical issue for current mode controlling, when it operates in higher than 50% of the duty-cycle. In FS6107D the slope compensation circuit is integrated by adding voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

● Leading Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs across the sensing resistor. The spike is caused by primary side capacitance and secondary side capacitance and secondary side rectifier reverse recovery. To avoid premature termination of the switching pulse, an internal leading edge blanking circuit is built in. During this blanking period (250ns, typical), the PWM comparator is disabled and cannot switch off the gate driver.

● Green Mode Operation

Since the main power dissipation at light/zero load in a switching mode power supply is from the switching loss which is proportional to the PWM switching frequency. To meet green mode requirement, it is necessary to reduce the switching cycles under such conditions either by skipping some switching pulses or by reducing the switching frequency.

● Smooth Frequency Foldback

In FS6107D, a Proprietary "Smooth Frequency Foldback" function is integrated to foldback the PWM

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switching frequency when the loading is light. Compared to the other frequency reduction implementations, this technique can reduce the PWM frequency smoothly without audible noise.

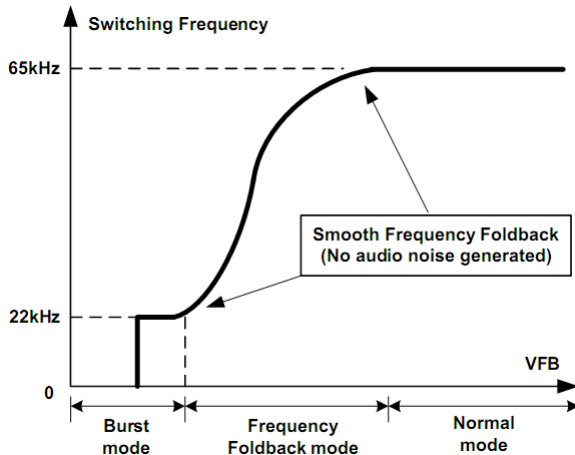


Fig.5

- **Burst Mode Control**

When the loading is very small, the system enters into burst mode. When VFB drops below V_{skip} , FS6107D will stop switching and output voltage starts to drop (as shown in Fig.6), which causes the VFB to rise. Once VFB rises above V_{skip} , switching resumes. Burst mode control alternately enables and disables switching, thereby reducing switching loss in standby mode.

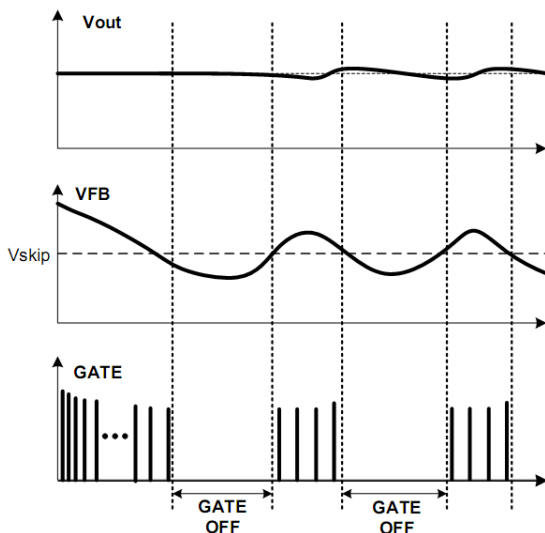


Fig.6

- **On Chip Thermal Shutdown (OTP)**

When the IC temperature is over $165\text{ }^{\circ}\text{C}$, the IC shuts down. Only when the IC temperature drops to $140\text{ }^{\circ}\text{C}$, IC will restart.

- **Soft Start**

FS6107D features an internal 20ms (typical) soft start that slowly increases the threshold of cycle-by-cycle current limiting comparator during startup sequence. It helps to prevent transformer saturation and reduce the stress on the secondary diode during startup. Every restart attempt is followed by a soft start activation.

- **Constant Power Limiting**

A proprietary “Constant Power Limiting” block is integrated to achieve constant maximum output power capability over universal AC input range. Based on the duty cycle information, the IC generates OCP threshold according to a proprietary analog algorithm.

- **Over Load Protection (OLP) in CV Mode**

In CV mode and if over load occurs, a fault is detected. If this fault is present for more than 75ms (typical), the protection will be triggered, the IC will experience an auto-recovery mode protection as mentioned above. The 75ms delay time is to prevent the false trigger from the power-on and turn-off transient.

- **VDD Over Voltage Protection (OVP) and Zener Clamp**

When VDD voltage is higher than 31V (typical), the IC will stop switching. This will cause VDD fall down to be lower than VDD_OFF (typical 9V) and then the system will restart up again. An internal 35V (typical)

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zener clamp is integrated to prevent the IC from damage.

- **Auto Recovery Mode Protection**

As shown in Fig.7, once a fault condition is detected, PWM switching will stop. This will cause VDD to fall because no power is delivered from the auxiliary winding. When VDD falls to VDD_OFF (typical 9V), the protection is reset and the operating current reduces to the startup current, which causes VDD to rise. The system begins switching when VDD reaches to VDD_ON (typical 21V). However, if the fault still exists, the system will experience the above mentioned process. If the fault has gone, the system resumes normal operation. In this manner, the auto restart can alternatively enable and disable the switching until the fault condition is disappeared.

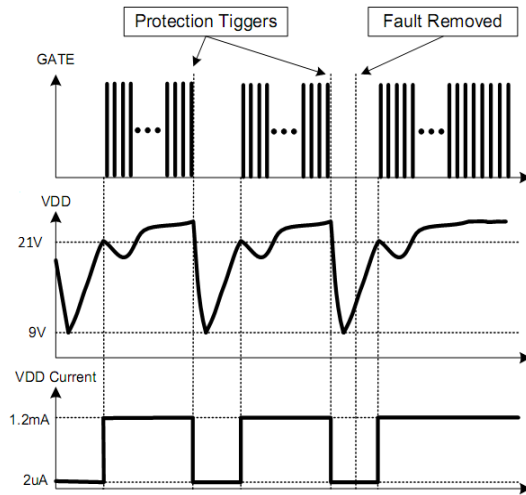
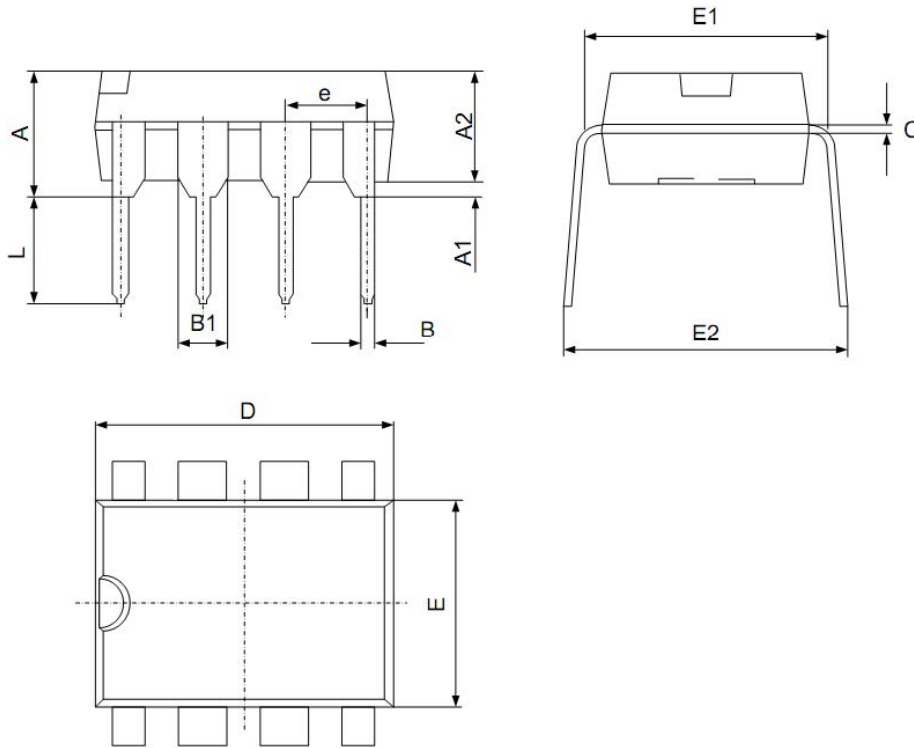


Fig.7

- **Soft Gate Driver**

The output stage of FS6107D is a totem-pole gate driver with optimized EMI performance. An internal gate clamp is added for MOSFET gate protection at higher than expected VDD input.

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■ Package Dimensions
DIP-8


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	5.334	0.146	0.210
A1	0.381		0.015	
A2	3.175	3.600	0.125	0.142
B	0.350	0.650	0.014	0.026
B1	1.524 (BSC)		0.06 (BSC)	
C	0.200	0.360	0.008	0.014
D	9.000	10.160	0.354	0.400
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.1 (BSC)	
L	2.921	3.810	0.115	0.150
E2	8.200	9.525	0.323	0.375